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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/876,742	06/07/2001	Toshiyuki Miyauchi	450100-03274	1867

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 05/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/876,742	MIYAUCHI ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 49-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 49-61* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claims 1-13 and 49-61 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 1 recites new matter: "**concurrent** operations of comparison, absolute value computation and selection in log likelihood computations". Claim 48 recites new matter: "**concurrent** operations of comparison, absolute value computation, and selection in log likelihood computations". The Examiner asserts that Figure 24 of the Applicant's disclosure teaches that absolute value computation and comparison operations take place concurrently and that selection of comparison results occurs concurrently with selection of absolute value computation results. However nowhere in the specification does the Applicant teach that selection can occur concurrently with the comparison and absolute value computation. In fact, the Applicant teaches that selection of comparison results and selection of absolute value computation results require output of from the absolute value computation and comparison operations and hence the Applicant explicitly teaches that

selection **cannot** occur concurrently with the comparison and absolute value computation.

Specification

2. The disclosure is objected to because of the following informalities: Claim 48 recites new matter: "**concurrent** operations of comparison, absolute value computation, and selection in log likelihood computations". The Examiner asserts that Figure 24 of the Applicant's disclosure teaches that absolute value computation and comparison operations take place concurrently and that selection of comparison results occurs concurrently with selection of absolute value computation results. However **nowhere in the specification** does the Applicant teach that selection can occur concurrently with the comparison and absolute value computation. In fact, the Applicant teaches that selection of comparison results and selection of absolute value computation results require output of from the absolute value computation and comparison operations and hence the Applicant explicitly teaches that selection **cannot** occur concurrently with the comparison and absolute value computation.

Appropriate correction is required.

Response to Arguments

3. Applicant's arguments filed 04/21/2005 have been fully considered but they are not persuasive.

The Applicant contends, "Van Stralen fails to teach or suggest a decoder including a path selection means configured to reduce the delay of the addition/comparison/selection (ACS) circuit in performing log-sum corrections by concurrently performing operations of comparison, absolute value computation, and selection in log likelihood computations, wherein the path selection means operates to generate corrections to the probability of the particular state of the Trellis diagram using at least two paths, one path showing a maximum likelihood and another path showing a second maximum likelihood, from at least three paths in the Trellis diagram. Further, Yamanaka was cited for teaching the user of concurrent operations of addition and comparison prior to selection in log likelihood computations. Therefore, it is maintained that Van Stralen and Yamanaka, individually or in combination fail to teach or suggest all the limitations of claim 1.

The Examiner disagrees and asserts that Figure 6 in Yamanaka teaches a path selection means configured to reduce the delay of the addition/comparison/selection (ACS) circuit in performing log-sum corrections by concurrently performing operations of comparison and absolute value computation (Note: col. 5, lines 63-67 in Van Stralen teach values are quantized to $64= 2^6$ levels, i.e., to 6 bits and since a 6 bit value is an element of the Galois Field, $GF[2^6]$ addition is identical to subtraction and addition is an absolute value computation; hence Yamanaka teaches concurrently performing operations of comparison and absolute value computation). Figure 5A in Van Stralen teach a path selection means comprising a multitude of addition/comparison/selection circuits 66 receiving alpha or Beta metrics for path selection in a Trellis (Note: alpha

metrics are forward path metrics and beta metrics are backward path metrics used in path selection; hence Van Stralen teaches the path selection means operates to generate corrections to the probability of the particular state of the Trellis diagram using at least two paths, one path showing a maximum likelihood and another path showing a second maximum likelihood, from at least three paths in the Trellis diagram).

All amendments and arguments by the applicant have been considered. It is the examiner's conclusion that the claims, as amended, are not patentably distinct or non-obvious over the prior art of record in view of the references, Van Stralen, Nick Andrew et al. (US 6304996 B1, hereafter referred to as Van Stralen), Yamanaka; Ryutaro et al. (US 6330684 B1) and Benedetto et al. (S. Benedetto, D. Divsalar, G. Montorsi, and F. Pollara, Soft-Output Decoding Algorithms in Iterative Decoding of Turbo Codes, TDA Progress Report 42-124, NASA Code 315-91-20-20-53) in view of XP-000888685 ("Simplified Log-Map Algorithm", Research Disclosure, Kenneth Mason Publications, Hampshire, GB, No. 421, May 1999, Page 612, ISSN: 0374-4353: Note this publication was provided by the Applicant in US Application 09/875310) as applied in the Final Action filed 03/11/2005. Therefore, the rejection is maintained.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 49-61 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claim 49 recites an abstract algorithm that can be carried out by hand or in a computer program with no tangible connection to hardware. Computer programs are non-statutory. Abstract algorithms are non-statutory.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-3 and 49-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Stralen, Nick Andrew et al. (US 6304996 B1, hereafter referred to as Van Stralen) in view of Yamanaka; Ryutaro et al. (US 6330684 B1).

See the Non-Final Action filed 03/11/2005 for detailed action of prior rejections.

6. Claims 4, 5, 52 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Stralen, Nick Andrew et al. (US 6304996 B1, hereafter referred to as Van Stralen) and Yamanaka; Ryutaro et al. (US 6330684 B1) in view of Benedetto et al. (S. Benedetto, D. Divsalar, G. Montorsi, and F. Pollara, Soft-Output Decoding Algorithms in Iterative Decoding of Turbo Codes, TDA Progress Report 42-124, NASA Code 315-91-20-20-53).

See the Non-Final Action filed 03/11/2005 for detailed action of prior rejections.

7. Claims 6, 9, 10, 12, 13, 54, 57, 58, 60 and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Stralen, Nick Andrew et al. (US 6304996 B1, hereafter referred to as Van Stralen), Yamanaka; Ryutaro et al. (US 6330684 B1) and Benedetto et al. (S. Benedetto, D. Divsalar, G. Montorsi, and F. Pollara, Soft-Output Decoding Algorithms in Iterative Decoding of Turbo Codes, TDA Progress Report 42-124, NASA Code 315-91-20-20-53) in view of XP-000888685 ("Simplified Log-Map Algorithm", Research Disclosure, Kenneth Mason Publications, Hampshire, GB, No. 421, May 1999, Page 612, ISSN: 0374-4353: Note this publication was provided by the Applicant in US Application 09/875310).

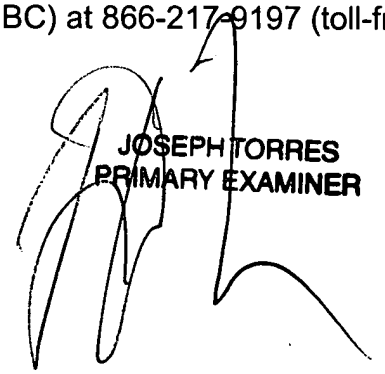
See the Non-Final Action filed 03/11/2005 for detailed action of prior rejections.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133